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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,664	07/26/2000	Ming Hung	004635.P001	6296

7590 05/19/2005

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EXAMINER

HYUN, SOON D

ART UNIT PAPER NUMBER

2663

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/625,664	<b>Applicant(s)</b> HUNG ET AL.	
	<b>Examiner</b> Soon D. Hyun	<b>Art Unit</b> 2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 November 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 2-10, 12-18 and 20-28 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 25-28 is/are allowed.
- 6) ☒ Claim(s) 2-7, 9-18, 20 and 21 is/are rejected.
- 7) ☒ Claim(s) 8 and 22-24 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 2-4, 9, 10-15, and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Beshai et al (U.S. Patent No. 6,721,271).

Regarding claim 2, Beshai et al (Beshai) discloses a system comprising:

a memory (N numbers of 66 in FIG. 7), wherein the memory includes a plurality of logical memories devices (66 in FIG. 7); and

a network switch (30 in FIG. 1) coupled to the memory, wherein the switch to write sequentially (according to predetermined order) a first portion of received packet data to a first of the plurality of logical memory devices and to write a second portion of the packet data to a second of the plurality of logical memory devices and to write a third portion of the packet data to a third of the plurality of logical memory devices (col. 10, line 48-col. 11, line 60).

Regarding claim 3, Beshai further discloses that the network switch further comprises a memory controller (ingress rotator or egress rotator 63 in FIG. 7)

Regarding claim 4, Beshai further discloses the ingress rotator and the egress rotator that are equivalent to a first memory controller component and a second memory controller component, respectively, as recited in the claims.

Regarding claim 9, Beshai discloses that the network switch further comprising:  
a receiver (an egress module 36 to receive data from the memory device))  
coupled to the memory controller;

a transmitter (an egress module 36 to transmit data to the outgoing links 42)  
coupled to the memory controller;

address resolution logic (inherently required to read and write data) coupled to  
the memory controller; and

packet queuing control (inherently required to store the data in the memory  
device) coupled to the memory controller, the receiver, the transmitter, and the address  
resolution logic.

Regarding claim 10, Beshai further discloses a media access controller (MAC)  
(an egress rate controller (FIG. 1).

Regarding claim 12, Beshai et al (Beshai) discloses a network switch (30 in FIG.  
1) comprising:

a first media access controller (MAC) (an egress module 36 in FIG. 1) coupled to  
a plurality of ports;

a receiver (an ingress module 32) coupled to the first MAC; and

a memory controller (ingress rotator 63 in FIG. 7) coupled to the receiver,  
wherein the memory controller to write a first portion of received packet data to a first of

the plurality of logical memory devices and to write a second portion of the packet data to a second of the plurality of logical memory devices and to write a third portion of the packet data to a third of the plurality of logical memory devices (col. 10, line 48-col. 11, line 60).

Regarding claims 20, Beshai discloses a method comprising:

receiving a first data packet at a network switch (30 in FIG. 1);

writing a first portion of the first data packet to a first logical memory device (first 66 in FIG. 7) coupled to the network switch;

writing a second portion of the first data packet to a second logical memory device (second 66 in FIG. 7) coupled to the network switch; and (col. 10, line 48-col. 11, line 60); and

writing a third portion of the first data packet to a third logical memory device (third 66 in FIG. 7) coupled to the network switch., wherein each writing step is performed in a first memory write access, respectively. See col. 10, line 48-col. 11, line 60.

Regarding claim 15, refer to the discussion for the claims 1, 4, and 12.

Regarding claim 21, Beshai further discloses a method comprising:

receiving a second data packet at the network switch; and

writing a first portion of the second data packet to the first logical memory device;

writing a second portion of the second data packet to the second logical memory device (col. 10, line 48-col. 11, line 60).

Regarding claims 13 and 14, refer to the discussion for the claims 12, 20, and 21.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 5-7 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beshai et al (U.S. Patent No. 6,721,271).

Regarding claims 5 and 16, Beshai et al (Beshai) does not explicitly teach that the first memory controller component and the second memory controller component access the corresponding logical memory devices via a shared address line. However, it would have been obvious to one having ordinary skill in the art to use a shared address line (bus) to simplify a circuit for a memory access.

Regarding claims 6, 7, 17 and 18, Beshai does not explicitly teach that the memory comprises SDRAMs and/or SSRAMs. However, it would have been obvious to one having ordinary skill in the art to use SDRAMs and/or SSRAMs for the memory to increase access speed.

***Allowable Subject Matter***

5. Claims 25-28 are allowed.

6. Claims 8 and 22-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter.

The prior art of record fails to teach that the memory controller maintains a record identifying a logical memory device that was last written to as cited in claim 8.

The prior art of record fails to teach the step of determining the logical memory device to which a portion of the first packet was last written as cited in claims 22 and 25.

The prior art of record fails to teach the step of writing the third portion of the data packet to both banks of the logical memory device if the size of the third portion of packet is less than a predetermined value as cited in claim 23.

### ***Response to Arguments***

8. Applicant's arguments filed 11/05/2004 have been fully considered but they are not persuasive.

Regarding claims 2 , 12 and 20, Applicant argues that the step of writing packet segments into logical memories by Beshai is not sequential, because the performing the writing packet segments into logical memories should be done during a single memory access as shown in FIG. 7. Examiner does not agree. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a single memory access) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, the FIG. 7

does not explicitly show that the writing is performed in the single write access.

Therefore, Examiner interprets the element as broad as possible such that the writing step is performed according to a predetermined order that is inherently required for the processing the step in the switch.

### ***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Soon D. Hyun whose telephone number is 571-272-3121. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.




Art Unit: 2663

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ly

S. Hyun  
05/12/2005

  
RICKY NGO  
PRIMARY EXAMINER 5/12/05